AMENDMENTS TO THE CLAIMS

This listing of claims will replace all prior versions and listings of claims in the application:

LISTING OF CLAIMS:

Claims 1- 59 (canceled).

60. (new): A circuit comprising:

a first switch rendered conductive and non-conductive in response to a first signal;

a second switch rendered conductive and non-conductive in response to a second signal;

a third switch rendered conductive when each of said first and second switches is rendered non-conductive; and

a capacitor coupled to said first, second and third switches such that said capacitor is brought into one of charging and discharging states through at least one of said first and second switches and into the other of the charging and discharging states through said third switch.

61. (new): The circuit as claimed in claim 60, wherein said first signal is different in phase from said second signal.

62. (new): The circuit as claimed in claim 61, further comprising a logic gate supplied with said first and second signals to produce a third signal, said third switch being rendered conductive and non-conductive in response to said third signal.

63. (new): The circuit as claimed in claim 62, wherein said logic gate comprises a NOR gate.

64. (new): The circuit as claimed in claim 60, further comprising a buffer circuit coupled to receive a charging and discharging voltage across said capacitor.

65. (new): The circuit as claimed in claim 62, wherein said first switch comprises a first transistor coupled between a first voltage node and a circuit node, said second switch comprising a second transistor coupled in parallel to said first transistor, said third switch comprising a third transistor coupled between said circuit node and a second voltage node, and said capacitor being coupled in parallel to said third transistor.

66. (new): A circuit comprising a first input terminal supplied with a first signal, a second input terminal supplied with a second signal, a first output terminal, a second output terminal, a third output terminal, and a timing control circuit coupled to said first and second input terminals and said first, second and third output terminals to produce at said first output terminal a first output signal relative to said first input signal, at said third output terminal a third output signal relative to said second input signal and at said second output terminal a second output signal that has a level changing edge appearing between a level changing edge of said first output signal and a level changing edge of said third output signal.

67. (new): The circuit as claimed in claim 66, wherein said timing control circuit comprises first, second and third unit circuits, each of said first, second and third unit circuits comprising:

first and second nodes,

a first switch rendered conductive and non-conductive in response to a signal supplied to said first node;

a second switch rendered conductive and non-conductive in response to a signal supplied to said second node;

a third switch rendered conductive when each of said first sand second switches is rendered non-conductive;

a capacitor coupled to said first, second and third switches such that said capacitor is brought into one of charging and discharging states through at least one of said first and second switches and into the other of the charging and discharging states through said third switch; and

a third node coupled to said capacitor;

said first terminal being coupled to said first and second nodes of said first unit circuit and said first node of said second unit circuit, said second terminal being coupled to said first and second nodes of said third unit circuit and said second node of said second unit circuit, and said first,

second and third output terminals being coupled respectively to the third n

ode of said first unit circuit, the third node of said second unit circuit and the third node of said third unit circuit.

68. (new): The circuit as claimed in claim 67, wherein each of said first, second and third unit circuits further comprises a logic gate coupled to the first and second node to control said third switch.

69. (new): The circuit as claimed in claim 68, wherein said logic gate comprises a NOR gate.

70 . The circuit as claimed in claim 67, wherein each of said first, second and third unit circuits further comprises a buffer circuit coupled between said capacitor and the third node.

71. The circuit as claimed in claim 70, wherein said first, second and third switches comprises first, second and third transistors, respectively, said first and second transistors being coupled in parallel to each other between a first voltage node and an input end of said buffer circuit, said third transistor and said capacitor being coupled in parallel to each other between the input end of said buffer circuit and a second voltage node.

72. (new): The circuit as claimed in claim 71, wherein said first transistor has a control gate coupled to said first node, said second transistor having a control gate couple to said second node, and said third transistor having a control gate coupled to an output end of a logic gate having first and second input ends coupled respectively to said first and second nodes.

73. (new): The circuit as claimed in claim 72, wherein said logic gate comprises a NOR gate.